Amendments to the Claims:

Claims 1 through 20 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon, sides and a back side;

at least one conductive ~~trace~~ lead frame member laterally spaced from ~~said~~ the at least one bond pad and having an upper surface and a lower surface, the lower surface of ~~said~~ the at least one conductive ~~trace~~ lead frame member having and inner end and an outer end and being substantially non-conductively attached to a portion of the active surface of ~~said~~ the semiconductor die and vertically spaced therefrom by a non-coextensive dielectric element interposed therebetween;

at least one discrete conductive bond connecting the inner end of the at least one conductive ~~trace~~ lead frame member to the at least one bond pad on the active surface of ~~said~~ the semiconductor die;

at least one carrier bond directly attached to the upper surface of the at least one conductive ~~trace~~lead frame member at the outer end thereof and extending transversely thereto; and

an encapsulant material disposed between the active surface of the semiconductor die and a portion of the lower surface of the at least one conductive lead frame member, extending over ~~encapsulating said~~ the sides and the back side of the semiconductor die, the outer end of the at least one conductive ~~trace~~lead frame member, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond ~~having~~ including another portion extending beyond ~~said~~ an outer surface of the encapsulant material.

2. (Currently Amended) A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of ~~said~~ the dielectric element attached to a portion of the active surface of ~~said~~ the semiconductor die;

a plurality of conductive ~~traces~~ lead frame members having inner ends laterally spaced from ~~said~~ the plurality of bond pads, each ~~trace~~ conductive lead frame member of the plurality of conductive ~~traces~~ lead frame members having an upper surface and a lower surface, a portion of the lower surface of each ~~trace~~ conductive lead frame member of ~~said~~ the plurality of conductive ~~traces~~ lead frame members being attached to a portion of the upper surface of ~~said~~ the dielectric element for connecting each conductive ~~trace~~ lead frame member of ~~said~~ the plurality of conductive ~~traces~~ lead frame members to the active surface of ~~said~~ the semiconductor die;

a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting the inner end of each conductive ~~trace~~ lead frame member of ~~said~~ the plurality of conductive ~~traces~~ lead frame members to at least one bond pad of the plurality of bond pads on the active surface of ~~said~~ the semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds directly disposed on the upper surface of each conductive ~~trace~~ lead frame member of ~~said~~ the plurality of conductive ~~traces~~lead frame members at a location remote from the inner end thereof and extending transversely from the upper surface thereof; and

an encapsulating material disposed about at least portions of ~~said~~ the semiconductor die, about ~~said~~ the dielectric element, between the active surface of the semiconductor die and the lower surface of a portion of each lead frame member of the ~~said~~ plurality of conductive ~~traces~~lead frame members, over outer ends of the lead frame members of the plurality, over ~~said~~ the plurality of discrete conductive bond members and over a portion of each carrier bond of ~~said~~ the plurality of conductive carrier bonds~~.~~, another portion of each carrier bond extending beyond an outer surface of the encapsulating material.

3. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the dielectric element includes an adhesive-coated polyimide tape.

4. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the dielectric element includes a polyimide film.

5. (Currently Amended) A chip-scale package as in claim 2, wherein the upper surface and lower surface of ~~said~~ the dielectric element are attached respectively to a portion of the lower surface of each conductive ~~trace~~ lead frame member of ~~said~~ the plurality of conductive ~~traces~~ lead frame members and a portion of the active surface of ~~said~~ the semiconductor die connecting portions of ~~said~~ the plurality of conductive ~~traces~~ lead frame members ~~and~~ to portions of ~~said~~ the active surface of the semiconductor die.

6. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive ~~traces~~ lead frame members comprises a plurality of lead fingers.

7. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive ~~traces~~ lead frame members comprises a conductive metal.

8. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of discrete conductive bond members comprises a conductive metal.

9. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of discrete conductive bond members comprises bond wires.

10. (Currently Amended) A chip-scale package as in claim 9, wherein ~~said~~ the bond wires comprise gold or aluminum.

11. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of discrete conductive bond members comprises TAB bonds.

12. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of discrete conductive bond members comprises thermocompression bonds.

13. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive carrier bonds includes metal.

14. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive carrier bonds is selectively located on the upper ~~surface~~ surfaces of ~~said~~ the plurality of conductive ~~traces~~ lead frame members, forming an array over the active surface of the semiconductor die.

16. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the plurality of conductive carrier bonds comprises solder balls.

17. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the encapsulating material comprises a substantially non-conductive material.

18. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~ the encapsulating material comprises a material having a low modulus of elasticity.

19. (Currently Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of ~~said~~ the plurality of conductive carrier bonds further comprises an upper portion and a lower portion, ~~said~~ the lower portion of ~~a~~ each conductive carrier bond being attached to the upper surface of ~~a~~ an associated conductive ~~trace~~ lead frame member of ~~said~~ the plurality of conductive ~~traces~~lead frame members.

20. (Currently Amended) A chip-scale package as in claim 19, wherein ~~said~~ the encapsulating material is disposed only about the lower portions of ~~said~~ the plurality of conductive carrier bonds.

21. (Withdrawn) A method for fabricating a chip-scale package comprising:

providing a semiconductor die having an active surface having at least one bond pad disposed thereon;

providing at least one conductive trace having an upper surface and a lower surface;

dielectrically attaching at least a portion of the lower surface of said at least one conductive trace to a portion of the active surface of said semiconductor die;

attaching a conductive bond member between said at least one conductive trace and the at least one bond pad disposed on the active surface of said semiconductor die;

attaching at least one carrier bond to a portion of the upper surface of said at least one conductive trace; and

encapsulating at least portions of said semiconductor die, said at least one conductive trace, said conductive bond and a portion of said at least one carrier bond.

22. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace as a lead frame element.

23. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace of a conductive metal.

24. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a wire bond.

25. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a TAB bond.

26. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond as a solder ball.

27. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond comprises an electrically conductive or conductor-filled polymer.

28. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, wherein said dielectrically attaching is effected using a polyimide tape.

29. (Withdrawn) A method for fabricating a chip-sized package as in claim 21, wherein the step of dielectrically attaching at least a portion of the lower surface of said conductive trace to a portion of the active surface of said semiconductor die further comprises:
providing a dielectric material having an upper surface and a lower surface;
attaching at least a portion of the lower surface of said joint material to at least a portion of the active surface of said semiconductor die; and
attaching at least a portion the lower surface of said at least one conductive trace to at least a portion of the upper surface of said joint material.